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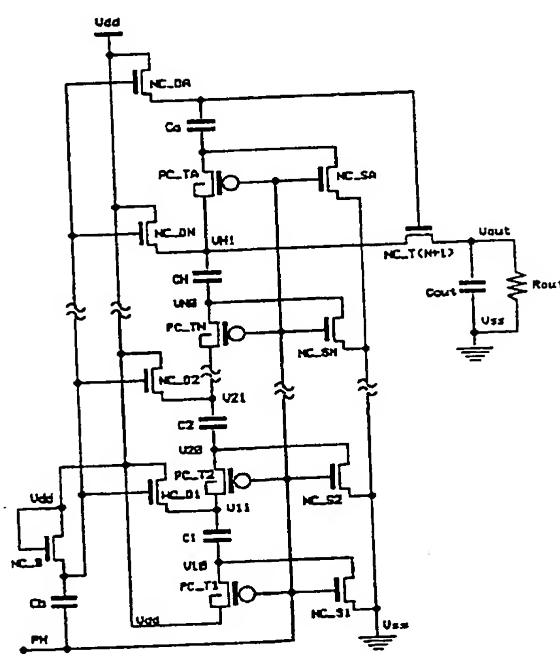
# (54) Improved on-chip voltage multiplier for semiconductor memories

(57) An on-chip voltage multiplier circuit, comprising N serially arranged stages wherein each stage includes a switch Tj (j = 1...N), having an upper pin and a lower pin, to the upper pin of which the lower pin of a capacitor Ci (i = 1 ... N) is serially connected, said capacitor also having a lower pin and an upper pin; the intermediate node between each switch Tj (j = 1 ...N) and each capacitor Ci (i = 1 ...N) is connected to the ground voltage Vss through a respective switch Si (i = 1 ...N) and the upper pin of each capacitor Ci (i = 1 ...N) is connected to the supply voltage Vdd through a switch Di (i = 1 ...N); and the lower pin of the switch (T1) of the first stage is directly connected to the supply voltage Vdd and the upper pin of the capacitor (CN) of the last stage is connected to the output pin through an additional switch (T(N + 1)).

FIG. 3



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**Descripti n**

This invention broadly relates to semiconductor memories and, more particularly, it relates to a novel implementation of a voltage multiplier circuit which enables integrated circuits manufactured in CMOS technology to be operated with a conventional supply voltage of 3.3 volts or 5.0 volts also in all those case wherein within the circuit and in certain circumstances, higher voltages are required.

It is well known, for instance, that, in addition to said conventional supply voltages of 5.0 or 3.3 volts, also higher voltages, that can be of 12 volts or even 18 volts, in certain circumstances are utilized in order to carry out programming or deleting operations on the memory cells. It is apparent that these memories, therefore, need an additional supply source, which is rather problematic, in the first place, due to the fact that the need to provide for two supply sources rather than simply one certainly is disadvantageous. The problem, therefore, is that a voltage higher than the supply voltage is to be provided on the chip.

This requirement has been satisfied at the present state of the art by utilizing particular approaches defined as "charge pumps" or by means of capacitor arrangements in "bootstrap" pattern, wherein the capacitors are charged in parallel and then are switched in series, so that the energy stored therein is utilized to raise the voltage.

The main drawback of this approach is that, when the load is increased, a voltage collapse occurs as a consequence of the fact that, of course, the situation is far from an ideal current generator.

By utilizing the approach of this invention, the voltage multiplication efficiency and the load current drive capability are noticeably improved with respect to the prior art approaches, particularly with respect to the charge pumps. Since the multiplication efficiency is strictly related to the power efficiency, this technique is also suitable for low power applications.

Further particulars and advantages as well as characteristics and construction details will be evident from the following description with reference to enclosed drawings wherein the preferred embodiments are shown by way of illustration and not by way of limitation.

In the drawings:

Figure 1 shows a Dickson voltage multiplier circuit with diodes,
Figure 2 shows a conceptual electric diagram of a voltage multiplier according to this invention, together with its related timing diagrams,
Figure 3 shows a circuit implementation with MOS transistors of the conceptual diagram of Figure 2,
Figure 4 shows a detailed circuit implementation of the voltage multiplier according to this invention,
Figure 5 shows a block diagram of a high voltage generator,
Figure 6 shows a two-module voltage multiplier circuit,
Figure 7 shows the results of a SPICE simulation on the circuit shown in Figure 6,
Figure 8 shows a further two-module, voltage multiplier circuit according to this invention,
Figure 9 shows the results of SPICE simulations on the circuit of Figure 8.

Most voltage multiplier circuits are based upon the diagram of Figure 1, which comprises two sets of parallel connected capacitors, driven by two phase signals PH and PH_, connected to and interdigitated with a serial diode chain, from the last of which the output current Iout is drawn at the desired voltage. Since diodes are not available in standard CMOS technology, a practical implementation of this circuit utilizes MOS transistors connected so as to operate as diodes. This high voltage generator directly incorporated with the chip (on-chip) was proposed by John Dickson in 1976 and it is basically derived from the Cockroft-Walton voltage multiplier. In the circuit shown in Figure 1, charge packets are pumped along the diode chain as the coupling capacitors are successively charged and discharged under action of the two clock signals PH and PH_ that are in antiphase relationship, with amplitude Vdd.

Assuming that the diodes are ideal, that the capacitors Ci (i = 1 .. N) have the same value and that the circuit is settled to the desired output voltage Vout with a constant average load current Iout, the following formulas apply:

$$\text{power efficiency} = \text{Vout}/[\text{Vdd} * (N + 1)] \quad (1)$$

$$N = \{ (\text{VNmax} - 2 * \text{Vdd}) / [\text{Vdd} - (\text{VNmax} - \text{Vout})] \} + 1 \quad (2)$$

wherein VNmax is the maximum voltage at the node VN before capacitor Cn discharges to the output.

Formula (1) means that the multiplication efficiency and the power efficiency, that is the ratio between the output power and the total supplied power, express the same concept. Normally, the diodes are replaced by N-channel MOS transistors connected to operate as diodes. P-channel transistors are not used because of difficulties associated with the substrate bias and with turning the devices off. Due to the poor capability of the N-channel MOS transistors to efficiently switch high voltage levels, the multiplication efficiency and the load current drive capability are both noticeably degraded with respect to the diode implementation. For example, a typical MOS transistor charge pump implementation

for generating a voltage of 18 volt from a 5 volt power supply has almost twice the stages needed for an equivalent diode implementation.

In order to overcome the above drawbacks, a first aspect of this invention suggests a novel technique for realising a voltage multiplier circuit, a conceptual electric diagram together with its related timings is shown in Figure 2.

As it can be seen from Figure 2, a number of serially arranged capacitors Ci (i = 1,...N) are provided interdigitated with a set of switches Tj (j= 2 ...N), the end and intermediate nodes of which are coupled to the supply voltage Vdd by means of a set of switches T1 and Di (i = 1 ...N) and to ground by means of a set of switches Si (i = 1 ...N), the output current being drawn from the last capacitor CN by means of a further switch T (N + 1).

The circuit operates by using a clock signal PH to turn on and off the switches Di, Si and Tj (i = 1 .. N; j = 1 .. N+1). Each capacitor Ci is charged to voltage Vdd directly by the power supply Vdd when switches Di and Si are on and switches Tj are off. In the next clock signal phase, switches Di and Si turn off and the switches Tj turn on. In such switching arrangement capacitors Ci are connected in series and are discharged directly to the output.

The minimum number N of capacitors should be used to exceed, by a reasonable value ΔV, the desired output voltage Vout. Assuming that capacitors Ci have the same capacitance value C and that F is the PH clock signal frequency and that the circuit is settled to the desired output voltage Vout with a constant average load current Iout, the following formulas apply:

$$\Delta V = Vdd * (N + 1) - Vout \tag{3}$$

$$Iout = \Delta V * C * F / N \tag{4}$$

As concerns the power efficiency, formula (1) is still valid. Since the value of N is equal, or almost equal, to the theoretical minimum value also in a practical implementation, the new voltage multiplier is suitable for low power applications, such as in circuits with battery power supplies.

Since the voltage across the switches Tj (j = 1 ... N) varies from 0 volts to Vdd and never changes in sign, these switches can be implemented with P-channel MOS transistors. Since a different bias configuration exists for switch T(N+1) as well as for switches Di, N-channel MOS transistors are used to accomplish the function of switches Di, Si and T (N + 1).

A first practical implementation of the conceptual scheme of Figure 2 is shown in Figure 3. A bootstrap technique has been used to properly drive the gates of the N-channel MOS transistors whose sources are not at Vss potential.

The transistors NC_Di (i = 1 .. N) ( N-channel MOS transistors) as employed for implementing switches Di of Figure 2, are switched by a voltage doubler, which is made by capacitor Cb and by transistor NC_B, connected as a diode. As it can be observed, capacitor Cb is inserted between the clock signal source PH and the gates of all transistors NC_Di while the diode transistor NC_B is inserted between said capacitor Cb and the voltage supply Vdd.

As it can be observed, the circuit can be ideally considered as divided into stages the components of which are all connected in analogous way. By considering the first stage (C1, T1, S1, D1 in Figure 1 and C1, PC_S1, NC_D1 in Figure 3) it can be seen that transistor PC_T1 is inserted between voltage Vdd and node V10 for coupling or connection to a first terminal (lower pin) of capacitor C1 and it has its gate coupled or connected to the gate of transistor NC_S1. This latter transistor is inserted with its source and drain between voltage Vss and said node V10. Transistor NC_D1 is inserted between a second terminal (upper pin) of capacitor C1 and voltage Vdd and it has its gate pin driven by phase signal PH through capacitor Cb.

As far as output transistor T(N +1) of Figure 2 is concerned, by referring to Figure 3 it can be observed that it is realized by an NMOS transistor designated NC_T(N + 1) inserted between the upper pin of capacitor CN of the last stage and the output and it has its gate pin driven by the upper pin of capacitor Ca of a supplementary stage.

In fact, aiming at efficiently switching transistor NC_T(N + 1) which is employed to implement switch T(N + 1) of Figure 2, a small stage has been added to the top of the structure, comprising an NMOS type transistor NC_DA a capacitor Ca, a PMOS type transistor PC_TA as well as a transistor NC_SA, analogously connected as in the previous stages. The dimensions of transistors NC_DA, PC_TA and NC_SA as well as the Ca capacitance value are smaller than those of the corresponding components of the other N stages.

Since this circuit enables the capacitors Ci (i = 1 .. N) to be fully charged to Vdd and directly discharged to the output, the load current drive capability is improved with respect to a standard charge pump of equivalent implementation. Moreover, it should be noted that, in contrast with the circuit of FIG. 1, the maximum voltage across each capacitor (except the output capacitor Cout) is only equal to the supply voltage Vdd.

In order to achieve a higher efficiency, some electrical engineering improvements can be made in the circuitry of Figure 3. Finally, the definitive scheme of a four-stage voltage multiplier circuit is shown in Figure 4. Some connections have been reviewed and rearranged to reduce the voltage stress across the gate oxide of transistors NC_SA, NC_S4, NC_S3 and NC_S2 as well as to decrease their sizes. On the other side, the sizes of the transistors should be kept as low as possible, in order to reduce the parasitic capacitance effects on the high-voltage nodes.

Transistor NC_DA provides a path to charge capacitor Ca and at the same time it enables transistor NC_T5 to be quickly and surely turned off at the begin of the charging phase. In the front section of the circuit, a further NMOS type transistor NC_B1 also inserted with its source and drain pins between capacitor Cb and voltage Vdd, but having its base driven by the voltage of the upper pin of capacitor C1 of the first stage, has been added in parallel to transistor NC_B of Figure 3 (designated as NC_BO in Figure 4), in order to fully charge capacitor Cb, thereby off-setting the threshold drop occurring across diode transistor NC_BO.

The voltage stress establishing across the gate oxide of the P-channel transistors located in the upper section of the circuit may be easily reduced by coupling their gates directly to Vdd or to a lower high-voltage node. For example, the gate pin of transistor PC_TA could be coupled to voltage Vdd or to the node V10_5 or to V15_5. Node V20_5 should not be used because in such case there would be a voltage less than 5 volt to turn on the transistor PC_TA.

Such a connection change does not affect the electrical functionality of the circuit. However, provided that the CMOS integrated circuit process limits are not exceeded, the gate pins of the P-channel transistors should be coupled to node VDPC (drive of P-channel transistors), as shown in Figure 4, in order to decrease the sizes of these transistors and at the same time to drive them into a deep conduction state during the discharge phase. If a connection change is required, the gate pin of the P-channel transistors is preferably coupled to voltage Vdd.

The highest voltage within this voltage multiplier circuit is directly related to the output voltage Vout. The output voltage should not be allowed to exceed the required output voltage. For example, if the output current Iout is low or null and/or the supply voltage accidentally increases above the normal range, the voltages in the upper section of the circuit, namely in its final stages, may exceed the process limits, thereby resulting into consequences that those skilled in the art can easily understand.

A practical high-voltage generator implementation scheme based upon the teachings up to now described is shown in Figure 5. Referring to Figure 5, it can be observed that an output voltage Vout limiter has been inserted between the voltage multiplier circuit and the load, in order to prevent dangerous and useless over-voltages within the voltage multiplier circuit. Furthermore, in order to make Vout as stable as possible, a feedback loop has been realized around the voltage multiplier circuit, comprising a voltage divider circuit and a voltage controlled oscillator (VCO) by which the clock signal is provided to the input of the voltage multiplier circuit.

According to formulas (3) and (4), the variation of the output voltage Vout due to a variation of the output current Iout may be minimized by suitably trimming the clock frequency F. The output current Iout and the frequency F are related by the simple formula $Iout = K * F$, where K is assumed as constant and given by

$$\{ [Vdd *(N + 1) - Voutd] * C \} / N$$

wherein Voutd is the desired output voltage.

If the circuit of Figure 4 is considered as a "module", a voltage multiplier circuit should be made by two or more modules connected in parallel to the output, provided that they use non-overlapping clock signals, in order to reduce the ripple voltage at the output as well as to increase the load current drive capability.

## EXAMPLES

Two examples will now be described, carried out by means of SPICE simulations based upon use of 4Mb DRAM memories by TEXAS INSTRUMENTS INC.. The SPICE simulations have been carried out using Vss = 0 volts and Vbb = -3 volt, with Vpp = 5 volt.

### Example 1.

| | | |
|---|---|---|
| Data: | Vdd = 5 volt | F = 10 MHz |
| Requirements: | Vout = 12 volt | Iout = 1 mA |

By using formula (3), N has been set to 2 and therefore $\Delta V$ is 3 volt. Two modules have been used to reduce any ripple effects. From formula (4), the capacitance of capacitor C should be (100/3) pF but, taking the transistor capacitance as well as the non-ideal charging and discharging conditions into account, the value of C has been increased by 14% and set to 38.0 pF. The resulting designed voltage multiplier circuit is shown in Figure 6. SPICE simulation results are

shown in Figure 7. The output impedance, in a large range around the operation point, is practically constant and less than 2900 Ohms.

Example 2.

| | | |
|---|---|---|
| Data: | Vdd = 5 volt | F = 10 MHz |
| Requirements: | Vout = 18 volt | Iout = 100 µA |

By using formula (3), N has been set to 4 and therefore ΔV is 7 volt. N = 3 is a possible but not recommended value because the tolerance for ΔV would be too small. For example, should voltage Vdd drop by 10%, the tolerance ΔV would be reduced to zero. Also in this case, two modules have been used in order to reduce the ripple effects. From formula (4), the capacitance of capacitor C should be 2.86 pF but, taking the transistor capacitance as well as the non-ideal charging and discharging conditions into account, the value of C has been increased by 26% and set to 3.6 pF. The correction factor is almost proportional to N. The resulting designed voltage multiplier circuit is shown in Figure 8. SPICE simulation results are shown in Figure 9. The output impedance, in a large range around the operation point, is practically constant and less than 59 Kohms.

PARASITIC CAPACITANCE

Assuming that poly-poly capacitors are used, an important aspect of them is the parasitic capacitance associated with each plate. The largest parasitic capacitance is the one existing between the bottom plate and the underlying layer, which is supposed to be an N-well diffusion whose terminal is electrically isolated. To estimate the parasitic capacitance value, the following process data (from the 256Kb Flash EEPROM 5 volt only) have been used: plate separation = 0.03 µm; oxide thickness from the bottom plate to the underlying layer = 1 µm.

Neglecting the parasitic capacitance associated with the upper plate and taking the effect of the N-well diffusion into account, whose terminal is floating, a parasitic capacitance from the bottom plate to voltage Vss has been added to each capacitor with a value of 2.5% of the capacitance of the capacitor itself.

The SPICE simulation results are summarized below.

Example 1.

| | |
|---|---|
| Vout = 12 volt | Iout = 1 mA. |

The following lines have been added to the input SPICE deck of the first example:

CL0 L5_0 VSS 950FF PC
CL1 L10_0 VSS 950FF PC
CL3 L15_0 VSS 25FF PC
CR0 R5_0 VSS 950FF PC
CR1 R10_0 VSS 950FF PC
CR3 R15_0 VSS 25FF PC

| RESULTS OF SPICE SIMULATIONS TABLE OF THE OUTPUT VOLTAGES | | | | |
|---|---|---|---|---|
| | I(load) | | | |
| | 0.0 mA | 0.5 mA | 1.0 mA | 1.5 mA |
| Vout values disregarding parasitic capacitances | 14.8 V | 13.5 V | 12.1 V | 10.6 V |
| Vout values with parasitic capacitances included | 14.6 V | 13.3 V | 11.9 V | 10.5 V |
| Output voltage variation | -0.2 V | -0.2 V | -0.2 V | -0.1 V |

<u>Example 2</u>

| | |
|---|---|
| Vout = 18 volt | Iout = 100 μA. |

The following lines have been added to the input SPICE deck of the second example:

```
CL0 L5_0 VSS 90FF PC
CL1 L10_0 VSS 90FF PC
CL2 L15_0 VSS 90FF PC
CL3 L20_0 VSS 90FF PC
CL4L25_0 VSS 5FF PC
CR0 R5_0 VSS 90FF PC
CRI R10_0 VSS 90FF PC
CR2 R15_0 VSS 90FF PC
CR3 R20_0 VSS 90FF PC
Ct4R25_0 VSS 5FF PC
```

| RESULTS OF SPICE SIMULATION TABLE OF THE OUTPUT VOLTAGES | | | | |
|---|---|---|---|---|
| | I(load) | | | |
| | 0.0 μA | 50 μA | 100 μA | 150 μA |
| Vout values disregarding parasitic capacitances | 24.0 V | 21.2 V | 18.4 V | 15.4 V |
| Vout values with parasitic capacitances included | 22.1 V | 19.5 V | 17.0 V | 14.2 V |
| Output voltage variation | -1.9 V | -1.7 V | -1.4 V | -1.2 V |

The preferred embodiment of this invention has been hereinbefore explained, but it should be understood that those skilled in the art can made variations and changes therein without departing from the scope of this invention.

## Claims

1. An on-chip voltage multiplier circuit, characterized in that it comprises N serially arranged stages and each stage includes a switch Tj (j = 1...N), having an upper pin and a lower pin, to the upper pin of which the lower pin of a capacitor Ci (i = 1 ... N) is serially connected, said capacitor also having a lower pin and an upper pin; in that the intermediate node between each switch Tj (j = 1 ...N) and each capacitor Ci (i = 1 ...N) is connected to the ground voltage Vss through a respective switch Si (i = 1 ...N) and the upper pin of each capacitor Ci (i = 1 ...N) is connected to the supply voltage Vdd through a switch Di (i = 1 ...N); and in that the lower pin of the switch (T1) of the first stage is directly connected to the supply voltage Vdd and the upper pin of the capacitor (CN) of the last stage is connected to the output pin through an additional switch (T(N + 1)).

2. A voltage multiplier circuit according to claim 1, characterized in that said switches Tj (j= 1 ...N), on the one hand, and said switches Si and Di (i = 1 ...N), on the other hand, are driven in push - pull relationship, so that, when said switches Tj (j = 1 ...N) are open and said switches Si and Di (i = 1 ...N) are closed said capacitors Ci (i = 1...N) are charged up to the supply voltage Vdd and, in the subsequent phase, said switches Tj (j = 1 ...N) are closed and said switches Si and Di (i = 1 ...N) are open, so that all capacitors Ci (i = 1 ...N) are serially connected and are directly discharged to the output.

3. A voltage multiplier circuit according to claim 1, characterized in that the number N of the stages is the minimum number which enables the output voltage Vout to be overcome by a value ΔV, based on the following formulas

$$\Delta V = Vdd \, . \, (N + 1) - Vout$$

$$Iout = \Delta V \, . \, C \, . \, F/N$$

where C is the common capacitance value of said capacitors Ci (i = 1 ...N), F is the clock frequency and Iout is the average load current.

4. A voltage multiplier circuit according to preceding claims 1 to 3, characterized in that said switches Tj (j = 1 ...N) are implemented by means of P-channel MOS transistors (PC_T1, ...PC_TN) and said switches Di (i = 1 ...N), said switches Si (i = 1 ...N) as well as said additional switch (T(N + 1)) are implemented by means of N-channel MOS transistors (NC_D1, ...NC_DN; NC_S1 ...NC_SN; NC_T(N + 1)).

5. A voltage multiplier circuit according to claim 4, characterized in that the substrate of all P-channel transistors is connected to the source pin or to the drain pin whichever is at higher voltage.

6. A voltage multiplier circuit according to claim 4, characterized in that said N-MOS transistors employed to implement said switches Di (i = 1 ...N) are driven by a voltage doubler circuit comprising a capacitor (Cb) serially connected to a N-MOS transistor connected as a diode, wherein said capacitor (Cb) is inserted between the clock signal source (PH) and the gate pins of all N-MOS transistors implementing said switches Di (i = 1 ...N), while said diode transistor (NC_B) is inserted between said capacitor (Cb) and the supply voltage.

7. A voltage multiplier circuit according to claims 5 and 6, characterized in that it includes an additional stage comprising an N-MOS transistor (NC_DA), a capacitor (Ca) having a lower pin and an upper pin, a P-MOS transistor (PC_TA) as well as an N-MOS transistor (NC_SA), all connected in analogous way as the corresponding components of the previous stages.

8. A voltage multiplier circuit according to claim 7, characterized in that the upper pin of said capacitor (Ca) of said additional stage is connected to the gate of said additional N-MOS transistor (NC_T(N + 1)).

9. A voltage multiplier circuit according to claim 6, characterized in that a further N-MOS transistor (NC_B1) is connected in parallel to said N-MOS transistor of said voltage doubler circuit, said further transistor being inserted with its source and drain pins between said capacitor (Cb) and the supply voltage Vdd and having its gate driven by the voltage of the upper pin of said capacitor (C1) of the first stage of the circuit.

10. A voltage multiplier circuit according to any one of the preceding claims and substantially as described in the specification and shown in the annexed drawings.

FIG. 1

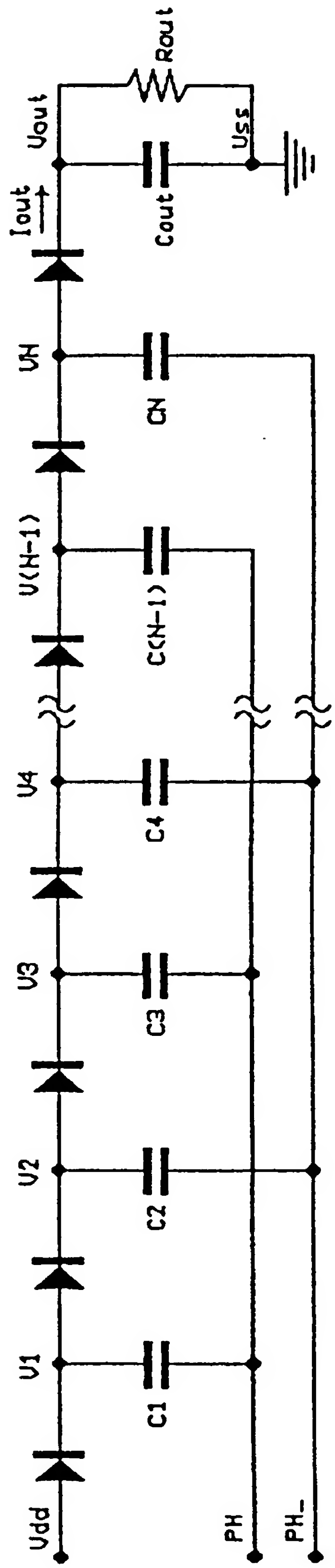

Rout
Vout
Iout
Cout
Vss
VN
CN
V(N-1)
C(N-1)
V4
C4
V3
C3
V2
C2
V1
C1
Vdd
PH
PH_

FIG. 2

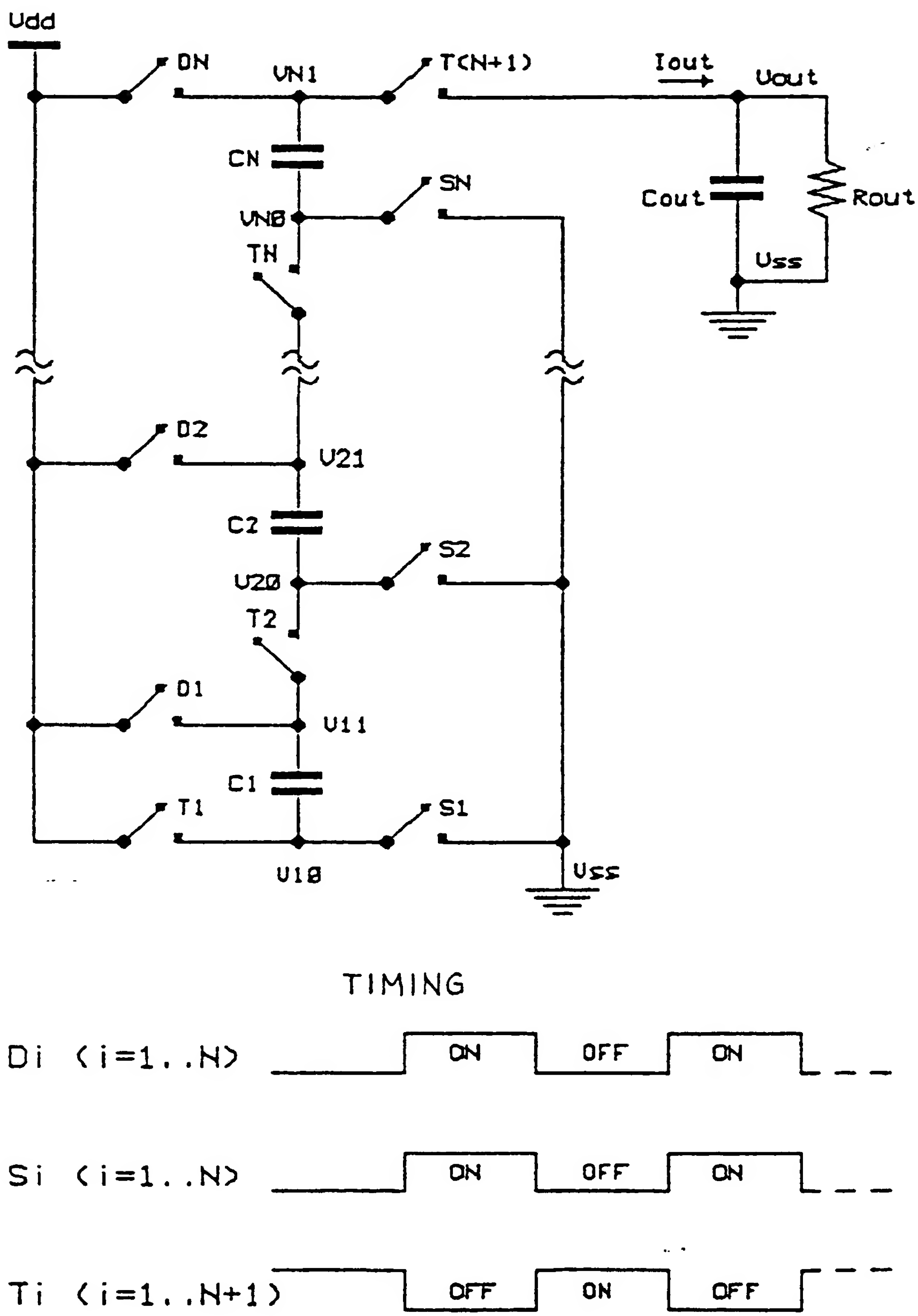
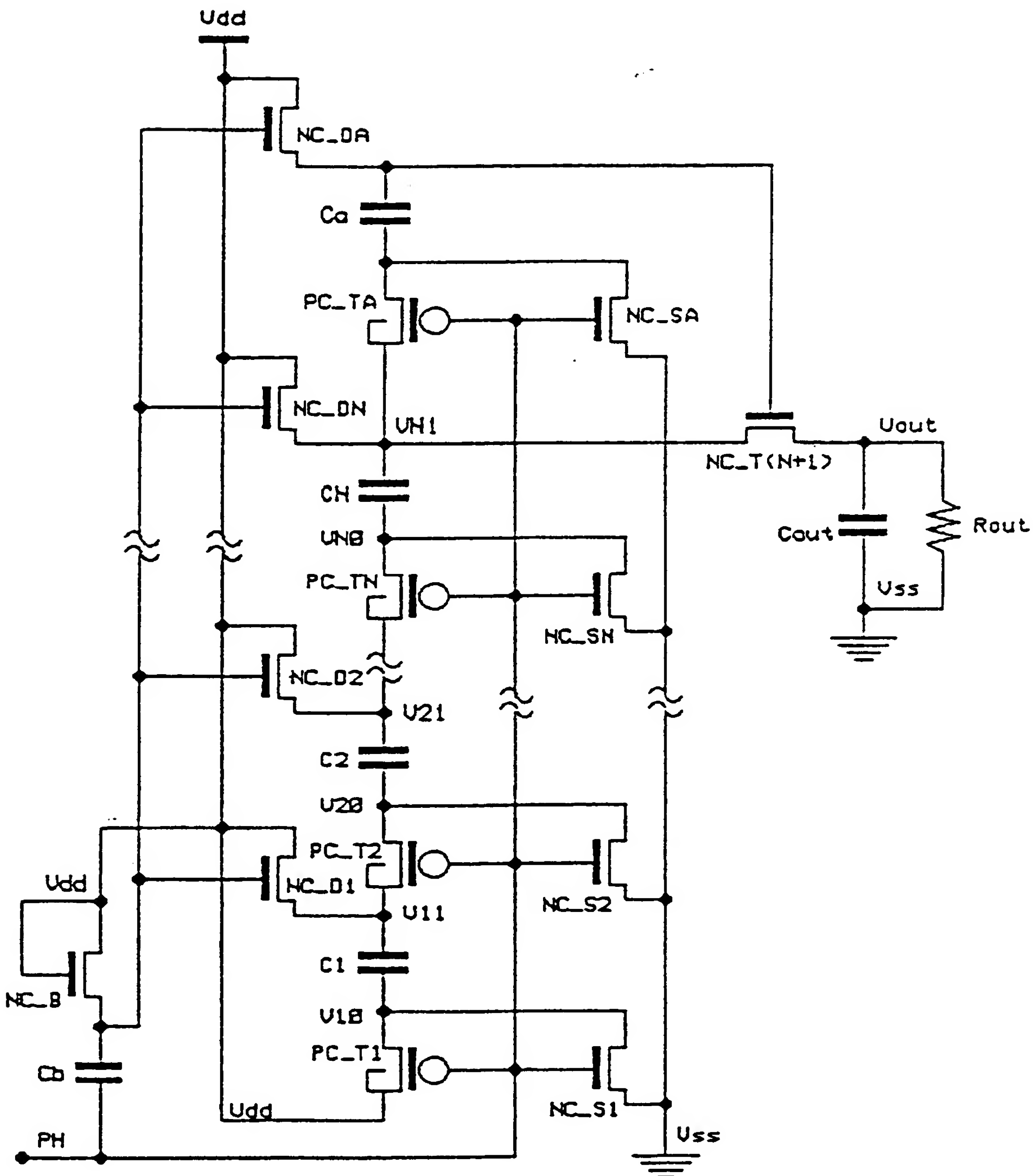

Udd
DN
VN1
T(N+1)
Iout
Uout
CN
SN
Cout
Rout
VN0
TN
Uss
D2
U21
C2
S2
U20
T2
D1
U11
C1
T1
S1
U10
Uss
TIMING
Di (i=1..N)
ON
OFF
ON
Si (i=1..N)
ON
OFF
ON
Ti (i=1..N+1)
OFF
ON
OFF

FIG. 3


Vdd
NC_DA
Ca
PC_TA
NC_SA
NC_DN
VH1
NC_T(N+1)
Vout
CH
VNB
PC_TN
NC_SN
Cout
Rout
Vss
NC_D2
V21
C2
V20
PC_T2
NC_S2
Vdd
NC_D1
V11
NC_B
C1
V10
PC_T1
NC_S1
Cb
Vdd
PH
Vss

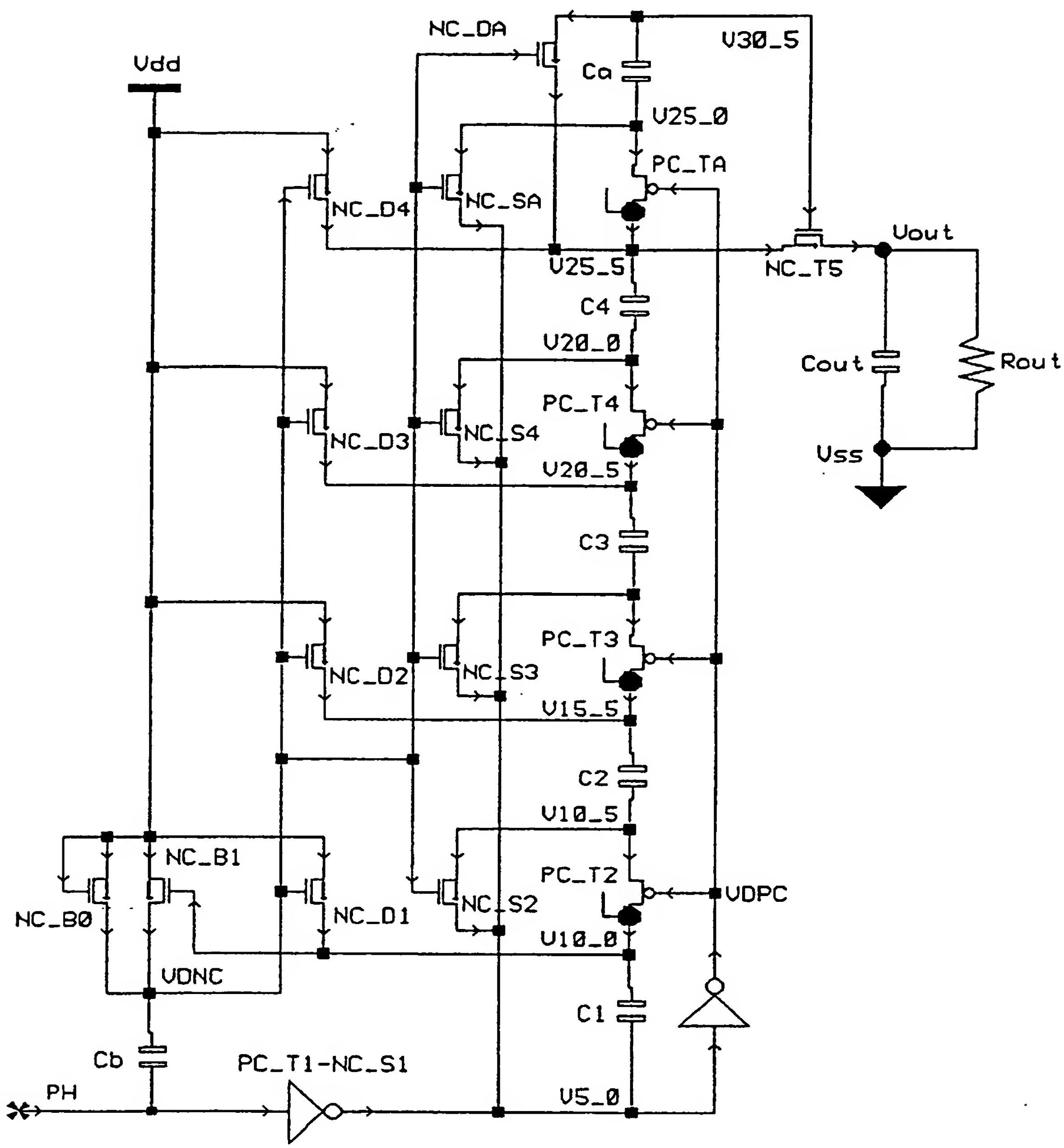

NC_DA
V30_5
Ca
Vdd
V25_0
PC_TA
NC_D4
NC_SA
Vout
V25_5
NC_T5
C4
V20_0
Cout
Rout
PC_T4
NC_D3
NC_S4
Vss
V20_5
C3
PC_T3
NC_D2
NC_S3
V15_5
C2
V10_5
NC_B1
PC_T2
VDPC
NC_B0
NC_D1
NC_S2
V10_0
VDNC
C1
Cb
PC_T1-NC_S1
PH
V5_0

FIG. 4

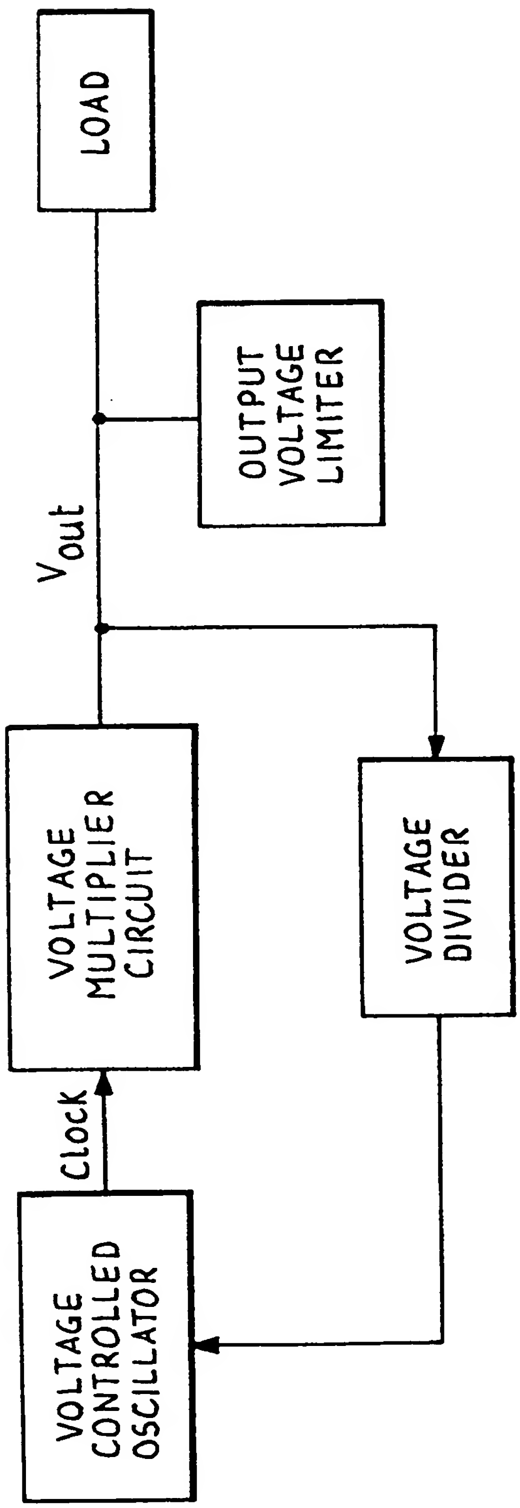

LOAD
OUTPUT VOLTAGE LIMITER
Vout
VOLTAGE MULTIPLIER CIRCUIT
VOLTAGE DIVIDER
Clock
VOLTAGE CONTROLLED OSCILLATOR

FIG. 5

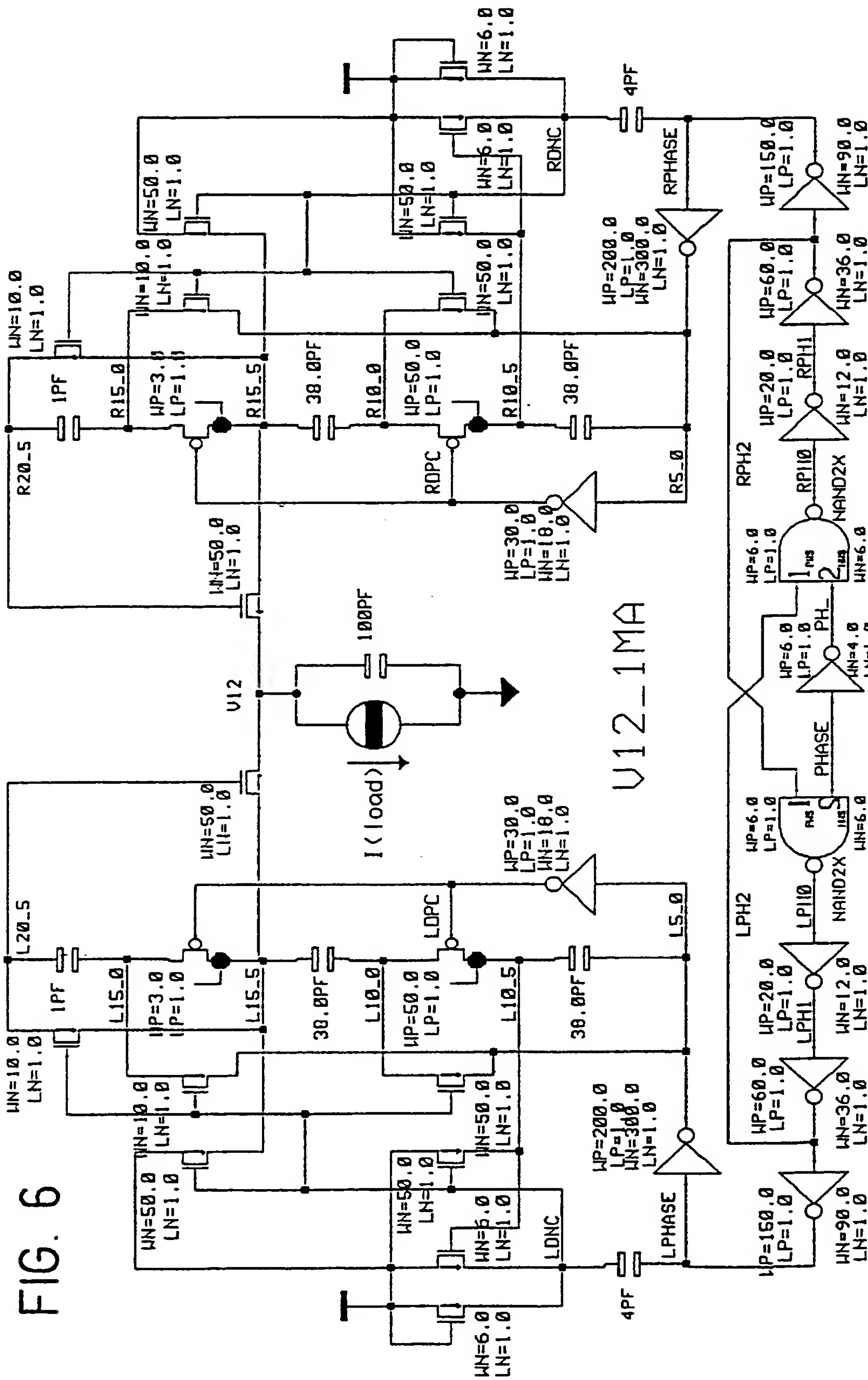

V12_1MA
V12
100PF
I(load)
RPHASE
LPHASE
RDNC
LDNC
RDPC
LDPC
R20_5
R15_0
R15_5
R10_0
R10_5
R5_0
L20_5
L15_0
L15_5
L10_0
L10_5
L5_0
1PF
30.0PF
4PF
RPH1
RPH2
RPI10
LPH1
LPH2
LPI10
NAND2X
INVX
PHASE
PH_
WN=6.0
LN=1.0
WN=50.0
WN=10.0
WP=3.0
LP=1.0
WP=50.0
WP=30.0
WN=10.0
WP=200.0
WN=300.0
WP=150.0
WN=90.0
WP=60.0
WN=36.0
WP=20.0
WN=12.0
WP=6.0
WN=4.0

FIG. 6

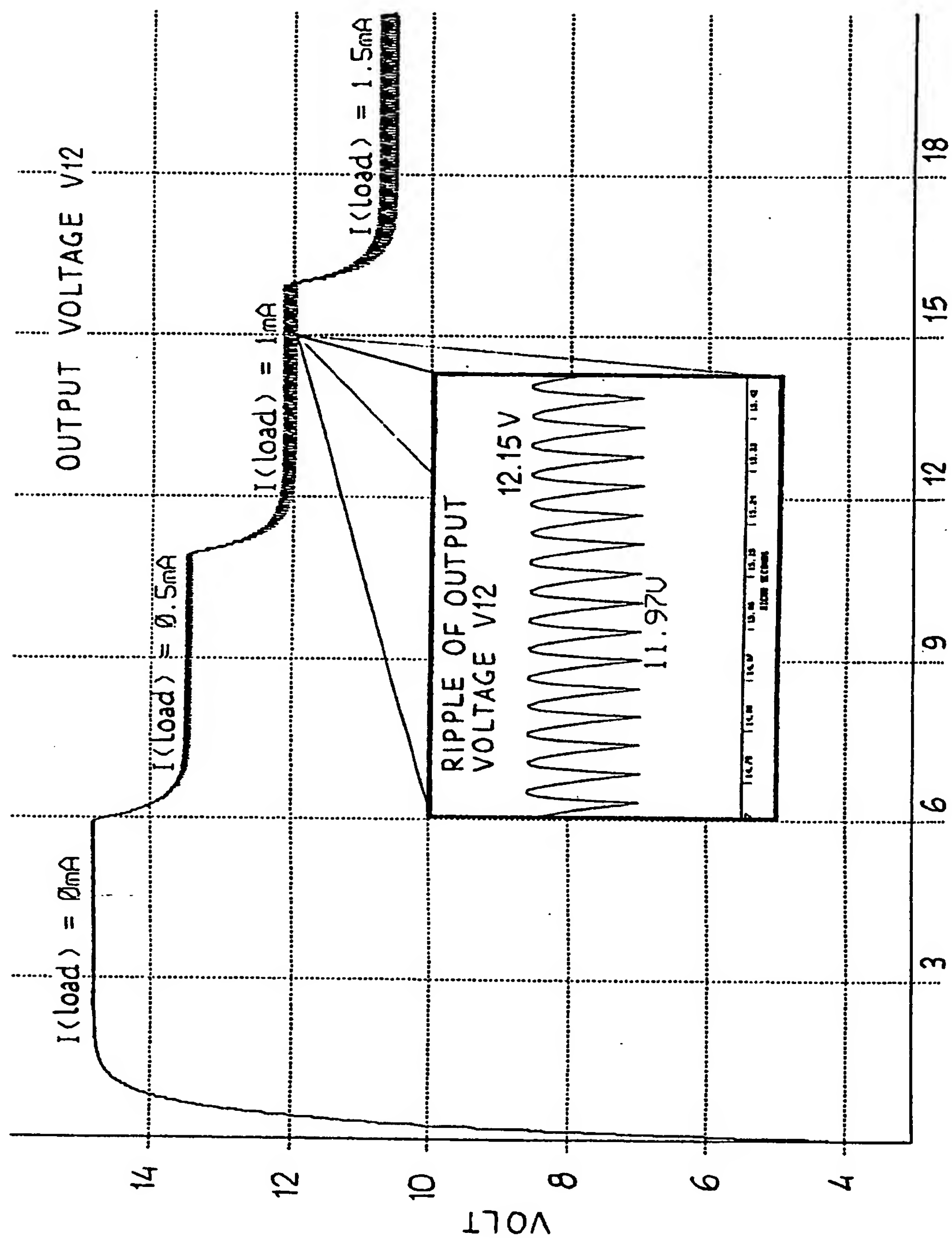
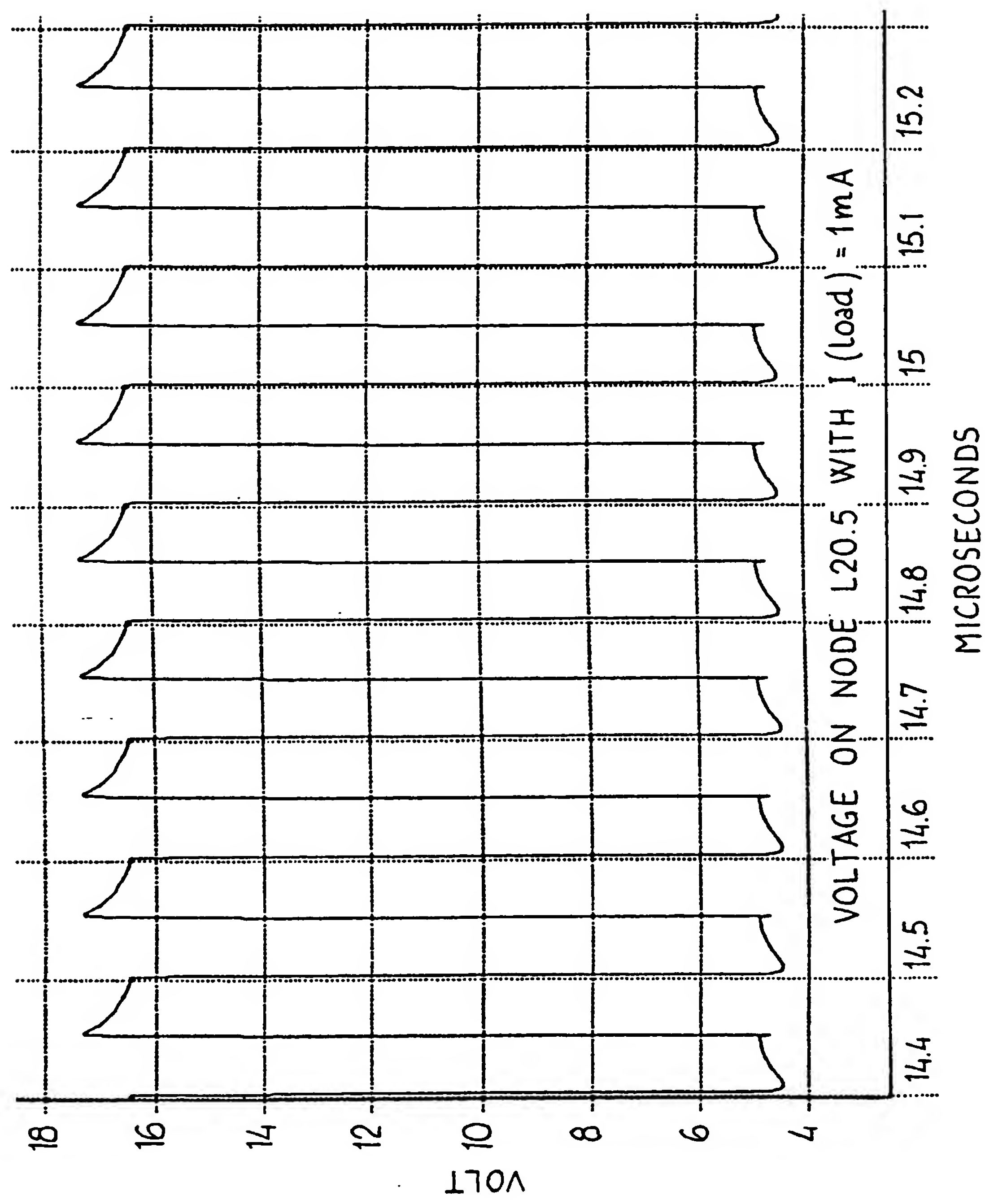

OUTPUT VOLTAGE V12
I(load) = ØmA
I(load) = Ø.5mA
I(load) = 1mA
I(load) = 1.5mA
RIPPLE OF OUTPUT VOLTAGE V12
12.15 V
11.97V
VOLT
14
12
10
8
6
4
MICROSECONDS
3
6
9
12
15
18

FIG. 7

FIG. 7(cont.)


VOLTAGE ON NODE L20.5 WITH I (Load) = 1mA
MICROSECONDS
14.4
14.5
14.6
14.7
14.8
14.9
15
15.1
15.2
VOLT
18
16
14
12
10
8
6
4

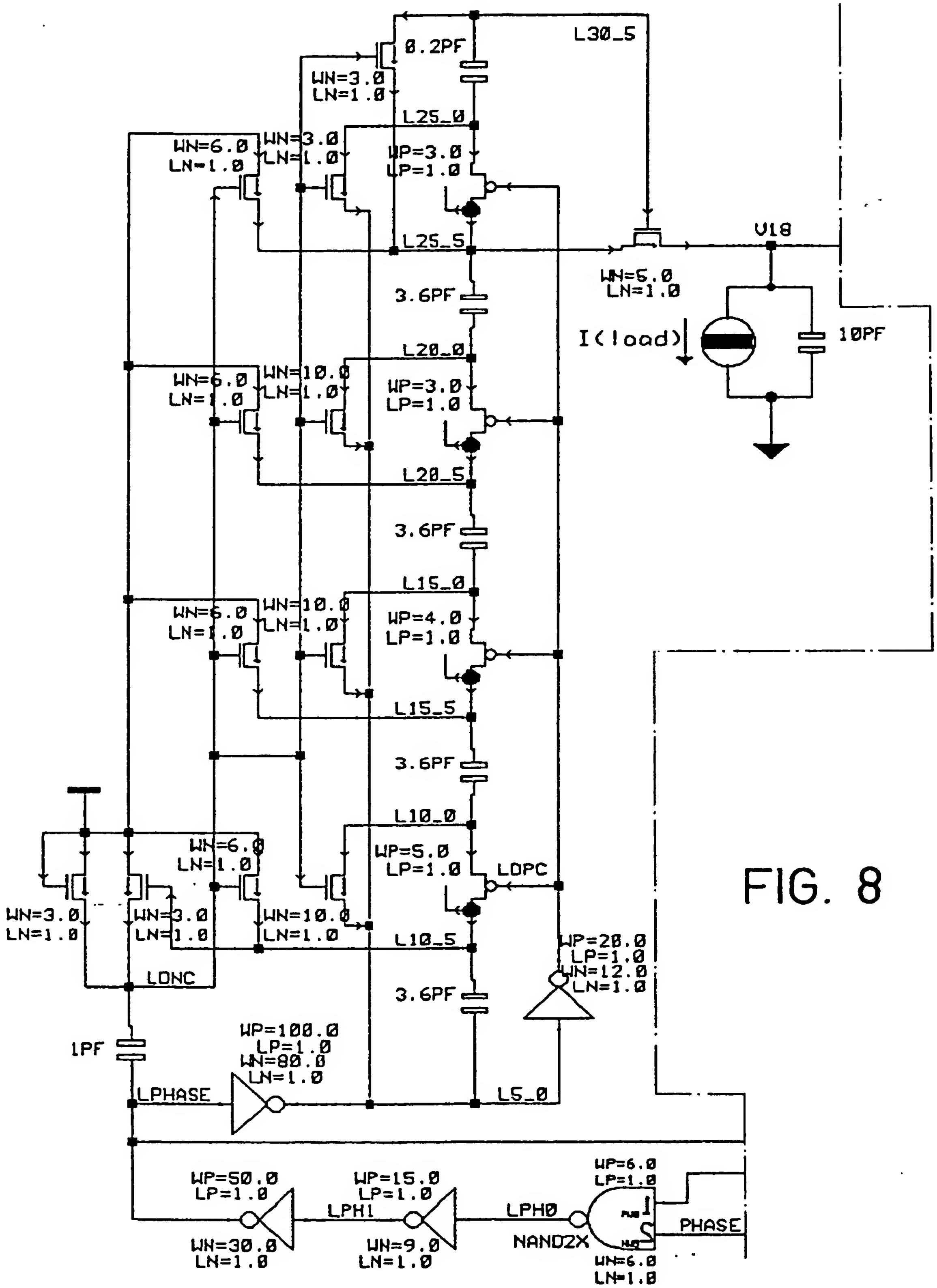

L30_5
0.2PF
WN=3.0
LN=1.0
L25_0
WN=6.0
LN=1.0
WN=3.0
LN=1.0
WP=3.0
LP=1.0
L25_5
V18
WN=5.0
LN=1.0
I(load)
10PF
3.6PF
L20_0
WN=6.0
LN=1.0
WN=10.0
LN=1.0
WP=3.0
LP=1.0
L20_5
3.6PF
L15_0
WN=6.0
LN=1.0
WN=10.0
LN=1.0
WP=4.0
LP=1.0
L15_5
3.6PF
L10_0
WN=6.0
LN=1.0
WP=5.0
LP=1.0
LDPC
WN=3.0
LN=1.0
WN=3.0
LN=1.0
WN=10.0
LN=1.0
L10_5
WP=20.0
LP=1.0
WN=12.0
LN=1.0
LDNC
3.6PF
1PF
WP=100.0
LP=1.0
WN=80.0
LN=1.0
LPHASE
L5_0
WP=50.0
LP=1.0
WN=30.0
LN=1.0
WP=15.0
LP=1.0
LPH1
WN=9.0
LN=1.0
LPH0
NAND2X
WP=6.0
LP=1.0
WN=6.0
LN=1.0
PHASE

FIG. 8

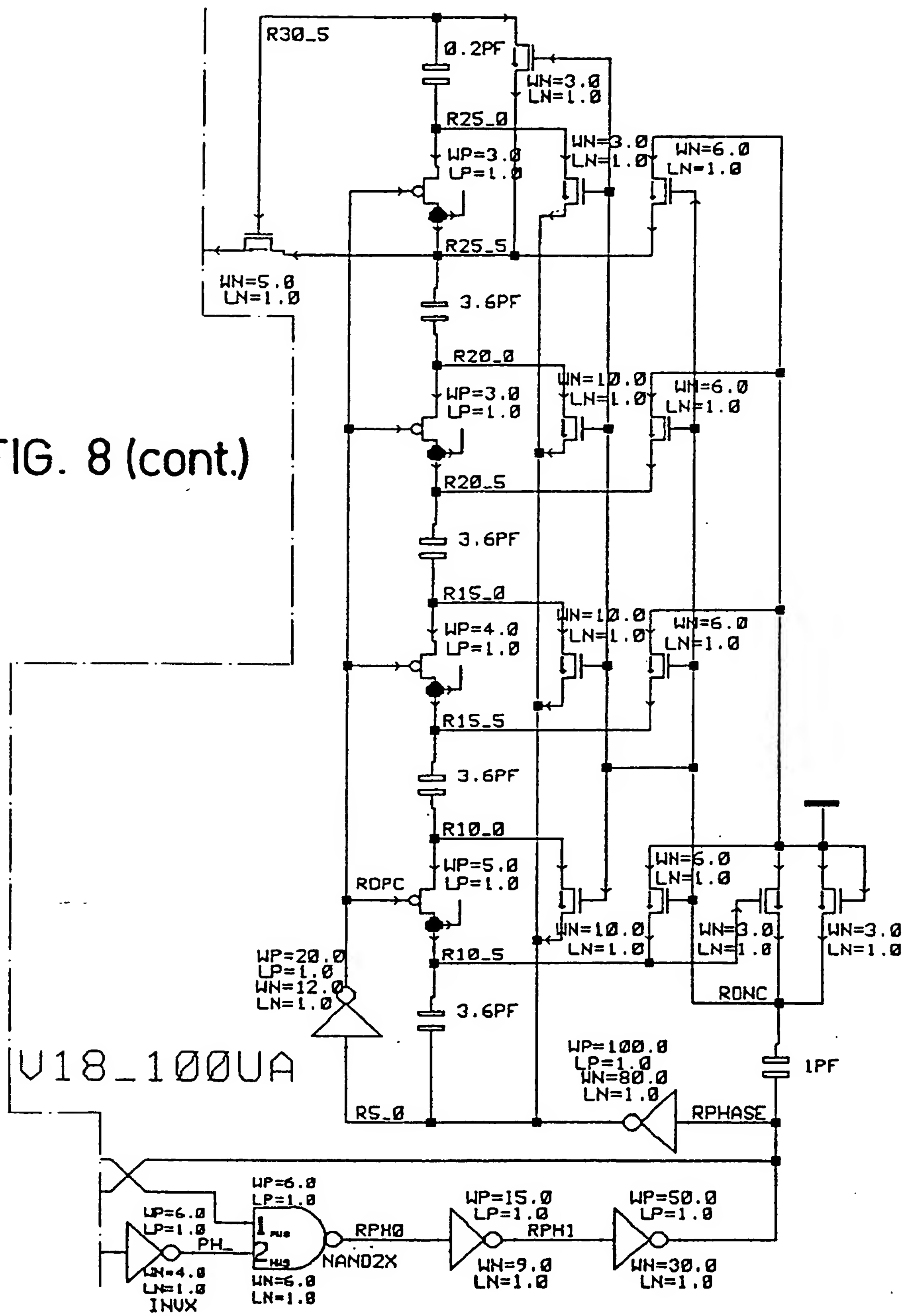

R30_S
0.2PF
WN=3.0
LN=1.0
R25_0
WP=3.0
LP=1.0
WN=3.0
LN=1.0
WN=6.0
LN=1.0
R25_S
WN=5.0
LN=1.0
3.6PF
R20_0
WP=3.0
LP=1.0
WN=10.0
LN=1.0
WN=6.0
LN=1.0
R20_S
3.6PF
R15_0
WP=4.0
LP=1.0
WN=10.0
LN=1.0
WN=6.0
LN=1.0
R15_S
3.6PF
R10_0
WP=5.0
LP=1.0
RDPC
WN=6.0
LN=1.0
WN=10.0
LN=1.0
WN=3.0
LN=1.0
WN=3.0
LN=1.0
R10_S
WP=20.0
LP=1.0
WN=12.0
LN=1.0
RDNC
3.6PF
V18_100UA
WP=100.0
LP=1.0
WN=80.0
LN=1.0
1PF
R5_0
RPHASE
WP=6.0
LP=1.0
WP=6.0
LP=1.0
PH_
WN=4.0
LN=1.0
INVX
RPH0
NAND2X
WN=6.0
LN=1.0
WP=15.0
LP=1.0
RPH1
WN=9.0
LN=1.0
WP=50.0
LP=1.0
WN=30.0
LN=1.0

FIG. 8 (cont.)

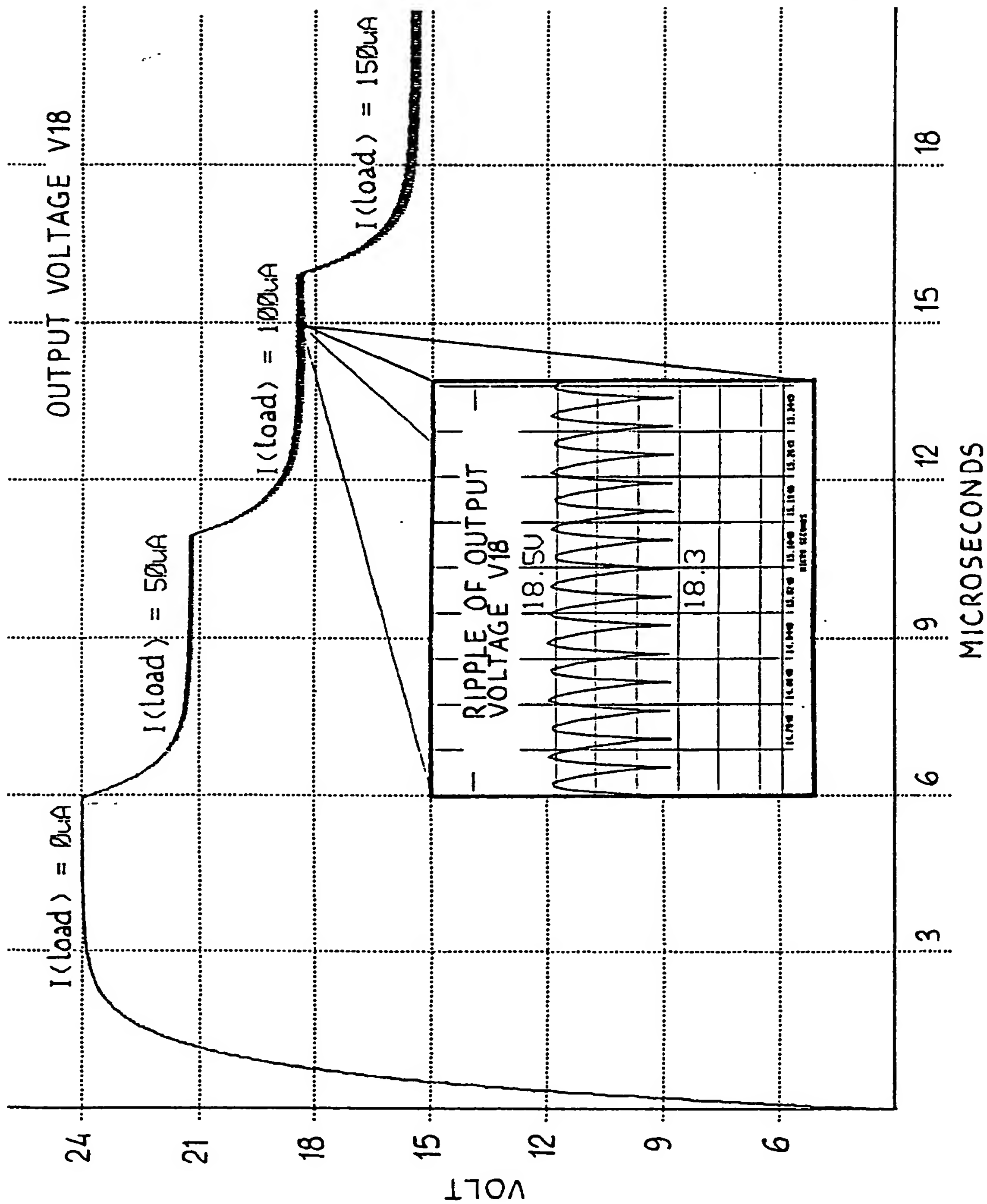
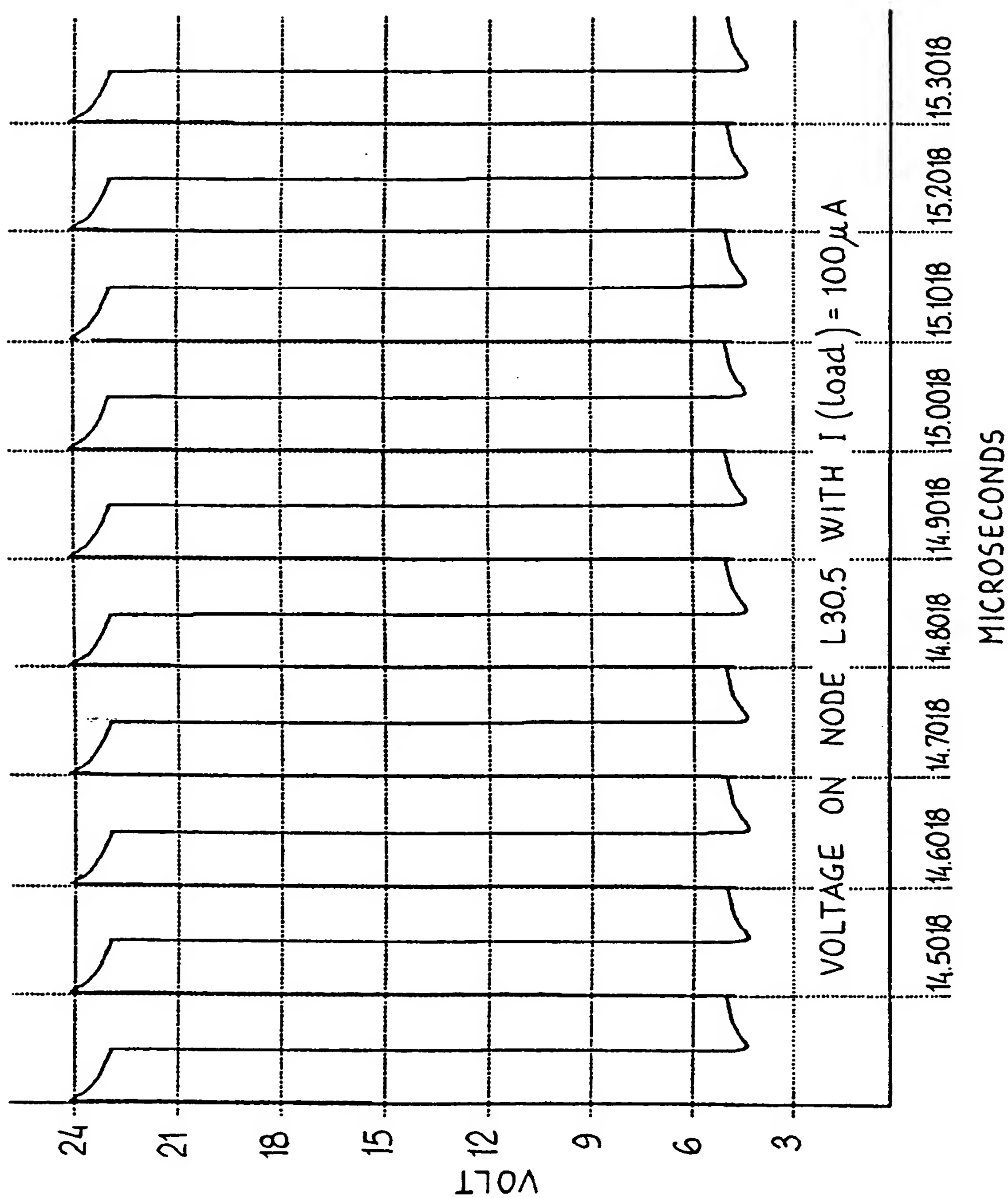

OUTPUT VOLTAGE V18
I(load) = ØuA
I(load) = 5ØuA
I(load) = 1ØØuA
I(load) = 15ØuA
RIPPLE OF OUTPUT VOLTAGE V18
18.5U
18.3
VOLT
24
21
18
15
12
9
6
MICROSECONDS
3
6
9
12
15
18

FIG. 9

FIG. 9(cont.)


VOLTAGE ON NODE L30.5 WITH I (Load) = 100μA
MICROSECONDS
VOLT
24
21
18
15
12
9
6
3
14.5018
14.6018
14.7018
14.8018
14.9018
15.0018
15.1018
15.2018
15.3018